IN THE CLAIMS:

Claims 16-37 and 46-51 were previously cancelled. Claim 1 has been amended herein. All of the pending claims are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

Listing of Claims:

1. (Currently amended) A process for reconstructing a semiconductor wafer, comprising:

forming at least a first alignment droplet and at least a second alignment droplet from a flowable alignment material at laterally spaced locations on a substrate;

placing a first semiconductor die having at least one alignment cavity on a surface thereof, such that the at least one alignment cavity of the first semiconductor die makes contact with the at least a first alignment droplet and is positioned by surface tension thereof;

placing a second semiconductor die having at least one alignment cavity on a surface thereof, such that the at least one alignment cavity of the second semiconductor die makes contact with the at least a second alignment droplet and is positioned by surface tension thereof;

inducing the at least a first alignment droplet and the at least a second alignment droplet to at least partially solidify to maintain positions of the first semiconductor die and the second semiconductor die; and

subsequently introducing an underfill material between the surfaces of the first and second semiconductor dice and the substrate to substantially fill a volume between each of the first and second semiconductor dice and the substrate, to extend laterally between the first and second semiconductor dice and to surround the at least a first alignment droplet and the at least a second alignment droplet to form a reconstructed semiconductor wafer.

2. (Previously presented) A process for reconstructing a semiconductor wafer, comprising:

forming at least a first alignment droplet and at least a second alignment droplet from a flowable alignment material at laterally spaced locations on a substrate comprising extruding the flowable alignment material through at least a first alignment via and at least a second alignment via to form the at least a first alignment droplet and the at least a second alignment droplet;

placing a first semiconductor die having at least one alignment cavity on a surface thereof, such that the at least one alignment cavity of the first semiconductor die makes contact with the at least a first alignment droplet and is positioned by surface tension thereof;

placing a second semiconductor die having at least one alignment cavity on a surface thereof, such that the at least one alignment cavity of the second semiconductor die makes contact with the at least a second alignment droplet and is positioned by surface tension thereof;

inducing the at least a first alignment droplet and the at least a second alignment droplet to at least partially solidify to maintain positions of the first semiconductor die and the second semiconductor die; and

subsequently introducing an underfill material adjacent the surfaces of the first and second semiconductor dice and surrounding the at least a first alignment droplet and the at least a second alignment droplet to form a reconstructed semiconductor wafer.

3. (Original) The process according to claim 2, wherein extruding the flowable alignment material through at least a first alignment via and at least a second alignment via to form at least a first alignment droplet and at least a second alignment droplet comprises extruding the alignment material from a supply of alignment material operably coupled to a reconstruction table.

4. (Original) The process according to claim 2, wherein the substrate comprises a fixture plate and wherein extruding the flowable alignment material through at least a first alignment via and at least a second alignment via to form at least a first alignment droplet and at least a second alignment droplet comprises extruding the flowable alignment material through alignment vias located in the fixture plate to form part of the reconstructed semiconductor wafer.

5. (Original) The process according to claim 1, wherein inducing the at least a first alignment droplet and the at least a second alignment droplet to at least partially solidify and maintain the positions of the first semiconductor die and the second semiconductor die comprises at least one of raising or lowering a temperature of the alignment material to at least partially solidify the alignment droplets.

6. (Original) The process according to claim 1, wherein inducing the at least a first alignment droplet and the at least a second alignment droplet to at least partially solidify and maintain the positions of the first semiconductor die and the second semiconductor die comprises reacting the alignment material with an activating agent to at least partially solidify the alignment droplets.

7. (Original) The process according to claim 1, wherein placing a first semiconductor die having at least one alignment cavity on a surface thereof, such that the at least one alignment cavity of the first semiconductor die makes contact with the at least a first alignment droplet and is positioned by the surface tension thereof comprises placing a semiconductor die having a plurality of alignment cavities on a surface thereof, each of the alignment cavities interacting with a correspondingly positioned alignment droplet to position the semiconductor die.

8. (Original) The process according to claim 7, wherein placing a semiconductor die having a plurality of alignment cavities on a surface thereof comprises placing a semiconductor die having a grid pattern of alignment cavities.

9. (Previously presented) The process according to claim 1, wherein introducing an underfill material between the surfaces of the first and second semiconductor dice and the substrate to substantially fill a volume between each of the first and second semiconductor dice and the substrate, to extend laterally between the first and second semiconductor dice and to surround the at least a first alignment droplet and the at least a second alignment droplet comprises introducing the underfill material between the first and second semiconductor dice and the substrate in the form of a fixture plate.

10. (Original) The process according to claim 1, further comprising curing the underfill material to a substantially solid state.

11. (Original) The process according to claim 1, further comprising singulating the first semiconductor die and the second semiconductor die from the reconstructed semiconductor wafer.

12. (Original) The process according to claim 11, wherein singulating the first semiconductor die and the second semiconductor die from the reconstructed semiconductor wafer comprises back-grinding the reconstructed semiconductor wafer to remove the underfill material.

13. (Original) The process according to claim 12, wherein back-grinding the reconstructed semiconductor wafer to remove the underfill material further comprises removing a fixture plate adhered to the underfill material by back-grinding the reconstructed semiconductor wafer.

14. (Original) The process according to claim 12, further comprising adhering active surfaces of the first semiconductor die and the second semiconductor die to an adhesive-coated film before singulating.

15. (Original) The process according to claim 14, further comprising removing the adhesive-coated film following the back-grinding.

16.-37. (Cancelled)

38. (Previously presented) A method of performing wafer-level processing on a number of separate semiconductor dice, the method comprising:

selecting a plurality of semiconductor dice;

forming at least one alignment via on a rear surface of each semiconductor die of the plurality;

positioning the semiconductor dice in proper positions wherein the alignment via of the rear surface of one semiconductor die is aligned with an alignment cavity of the mating semiconductor die to form a semiconductor wafer by placing the at least one alignment via in contact with corresponding alignment droplets positioned on a substrate and using surface tension of the alignment droplets to effect precise alignment of the semiconductor dice;

subsequently underfilling between the positioned semiconductor dice and the substrate to form a reconstructed semiconductor wafer; and

performing wafer-level processing on the reconstructed semiconductor wafer.

39. (Original) The method of claim 38, wherein selecting a plurality of semiconductor dice comprises selecting a number of known functional dice.

40. (Original) The method of claim 38, wherein positioning the semiconductor dice in proper positions to form a semiconductor wafer by placing the at least one alignment via in contact with corresponding alignment droplets further comprises inducing the alignment droplets to at least partially solidify to maintain the proper positions.

41. (Original) The method of claim 40, wherein inducing the alignment droplets to at least partially solidify to maintain the proper positions comprises at least one of raising or lowering a temperature of the alignment droplets.

42. (Original) The method of claim 38, wherein the substrate comprises a fixture plate and wherein positioning the semiconductor dice in proper positions to form a semiconductor wafer by placing the at least one alignment via in contact with corresponding alignment droplets comprises placing the at least one alignment via in contact with corresponding alignment droplets disposed on the fixture plate.

43. (Original) The method of claim 42, wherein underfilling the positioned semiconductor dice to form a reconstructed semiconductor wafer comprises introducing an underfill material between the rear surfaces of the semiconductor dice and a surface of the fixture plate.

44. (Original) The method of claim 38, wherein performing wafer-level processing on the reconstructed semiconductor wafer comprises performing a wafer-level testing operation on the reconstructed semiconductor wafer.

45. (Original) The method of claim 38, wherein performing wafer-level processing on the reconstructed semiconductor wafer comprises performing burn-in at the wafer level on the reconstructed semiconductor wafer.

46.-51. (Cancelled)